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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,943	06/22/2001	Takashi Udagawa	Q61743	6215

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/885,943	UDAGAWA, TAKASHI	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *16-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election of Group II (semiconductor device) claims 1-15 without traverse is acknowledged. Accordingly, claims 16-21 are herewith withdrawn from consideration.

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement filed on 6/22/01 and entered as Paper No. 3.

Drawings

1. Figure 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

In an invention in which the relative accuracy within which the stoichiometric parameters of compound semiconductor layers, in particular the light-emitting (GaN_xP_{1-x}) and buffer (BN_zP_{1-z}) layers, can be selected is crucial to the validity of the claims for which protection is sought, a discussion of the error bars (covariances) involved in (a) the empirical realization of said stoichiometric parameters (denoted as "x" and "z" above), and (b) the cited lattice constants of said light-emitting and buffer layers is a necessary condition for enablement. Said discussion is lacking in Applicant's disclosure

but should be included in a modified version of said disclosure. Appropriate action is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. ***Claims 6-9*** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In particular, claims 6-9 recite an accuracy of lattice matching, either as plus or minus ±0.4 % (claims 7-9, last sentence) or ±1.0% (claim 6, last sentence). However, applicant has not demonstrated nor discussed whether said accuracy can be empirically realized, and, if so, how. Therefore, said claims 6-9 lack enablement.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. ***Claim 1*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al (5,042,043) in view of Kawai (JP411045892A).

Hatano et al teach (front figure and title and abstract; in the latter on line 5 select the sub-range by selecting y=0 (no Al), and x=1 (no B); whereupon for future reference we shall adopt the notation of Applicant and denote the parameter "1-z" in Hatano et al by "x") a group III nitride semiconductor light-emitting device comprising a substrate 11 (column 4, lines 25-27) having thereon a light-emitting part structure comprising a gallium nitride phosphide single crystal layer 15 (column 4, lines 28-30) provided via a boron phosphide based buffer layer 13 (column 4, line 33). Hatano et al do not teach the said substrate to be a single crystal; however, Kawai teaches that for enhancing hardness and stability a single-crystal substrate is to be used in semiconductor light-emitting devices (see in English abstract, "Problem to be Solved"). Desirability of hardness and stability provides motivation; the inventions can be easily combined, as all that needs to be done is to select a single-crystal substance for the substrate material of choice.

6. ***Claims 2-3 and 5*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al and Kawai as applied to claim 1, and in further view of Thornton et al (6,372,356 B1).

With regard to claims 2 and 3: Neither Hatano et al nor Kawai teach the further limitations of claims 2 and 3. However, in the art of semiconductor substrate technology, specifically the technology that allows to grow lattice-mismatched high-quality crystals on top of each other (hence relevant to the art taught by Hatano et al and Kawai) Thornton et al teach an amorphous first buffer layer 320 (claim 2) for the purpose of releasing the underlying crystal layer (abstract, first sentence and column 2, lines 16-25)

with a crystalline buffer layer 314 on top of it (column 2, lines 16-25 and column 6, lines 39-50) so as to be able to comply or deform enough to allow lattice-mismatched layers to be grown on top of the crystalline buffer layer (claim 3). The teaching by Thornton et al can be combined with that of Hatano et al and Kawai by simply laminating the buffer layer in an amorphous lower part and a crystalline upper part, which teaching in no way interferes with the rest of the invention by Hatano et al and Kawai. Motivation is two-fold: the release of the crystalline substrate and the more gradual transition to the lattice structure planned on top of the buffer layer. The implementation of the teaching of Thornton et al in no way interferes with the rest of the invention as taught by Hatano et al and Kawai, and hence combining the inventions can reasonably be expected to be successful.

With regard to claim 5: the device taught by Hatano et al comprises a double hetero-junction structure as light-emitting part structure (see heterojunctions between layers 14 and 15, and between 15 and 16 (cf. column 4, line 35).

7. . ***Claim 4*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al and Kawai as applied to claim 1 above, and further in view of Liu et al (5,612,551). Neither Hatano et al nor Kawai necessarily teach the further limitation of *claim 4*. However, Liu et al teaches a single hetero-junction structure as light-emitting part of a light-emitting device for the purpose of making it unnecessary to use bandgap engineering to cope with the conduction band discontinuity between the light-emitting and collector layers (cf. column 1, lines 58-62). The problem exists also for Hatano et al, considering the discontinuity between the conduction bands of BP and $GaN_{1-x}P_x$. Hence

the teaching of Liu et al is relevant. The teachings can be combined, as all that is necessary is to remove enough hetero-junctions. Success can be reasonably expected as this removal does not interfere with the remainder of the teaching by Hatano et al and Kawai.

8. ***Claims 6, 9-10, and 13*** are under 35 U.S.C. 103(a) as being unpatentable over Hatano et al and Kawai as applied to claim 1 above, and further in view of Doll (5,326,424). Neither Hatano et al nor Kawai necessarily teach the further limitation defined by Applicant's claim 9. However, as shown by Doll (cf. title, abstract and column 4, lines 27-40) it has long been known in the art of boron nitride phosphide films in semiconductor devices that, for the specific purpose of enabling lattice matching of boron nitride phosphide layers with overlying semiconductor crystalline substrates the phosphor content in the boron nitride phosphide layer can be varied such as to cover the range between 3.6157(10) Å and 4.54 Å. Consequently, any stoichiometric value of the phosphorus content in the gallium nitride phosphide single crystal layer directly overlying the aforementioned boron nitride phosphide buffer layer that corresponds to a lattice constant of up to 4.54 (approximately corresponding to phosphorus concentrations up to 6%) can obviously be expected to be lattice-matched with said boron nitride phosphide buffer layer. Considering the teaching of matching the lattice of boron nitride phosphide layers to any crystalline layer with lattice constant between the limits as given in column 4, line 40, and considering that in the present application the overlying semiconductor layer itself is also a III-V compound semiconductor layer, hence has even more similarity with the aforementioned boron nitride phosphide buffer

layer than the silicon layer in Doll et al, it is particularly obvious that the teaching by Doll et al has not only motivation (lattice matching) but also combinability with reasonable expectation of success.

With regard to claims 10 and 13: Neither Hatano et al nor Kawai necessarily teach the further limitation as defined by claims 10 and 13, respectively. However, it is entirely obvious to limit the range of the stoichiometric parameter x defining the phosphorus concentration ratio ("compositional ratio") in the gallium nitride phosphide single crystal layer to maximally about 6% in view of the impossibility to raise the lattice constant of the underlying boron nitride phosphide buffer layer over the upper limit of the range indicated by Doll et al: no amount nor any lack of amount, of nitrogen or phosphorus in said boron nitride phosphorus buffer layer can be selected to achieve lattice matching for values of x for which the lattice constant of the gallium nitride phosphide single crystal layer exceeds that of boron phosphide.

9. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al, Kawai and Liu et al as applied to claim 4 above, and further in view of Doll (5,326,424). Neither Hatano et al, Kawai, nor Liu et al necessarily teach the further limitation defined by claim 7. However, as shown by Doll (cf. title, abstract and column 4, lines 27-40) it has long been known in the art of boron nitride phosphide films in semiconductor devices that, for the specific purpose of enabling lattice matching of boron nitride phosphide layers with overlying semiconductor crystalline substrates the phosphor content in the boron nitride phosphide layer can be varied such as to cover the range between 3.6157(10) Å and 4.54 Å. Consequently, any stoichiometric value of

the phosphorus content in the gallium nitride phosphide single crystal layer directly overlying the aforementioned boron nitride phosphide buffer layer that corresponds to a lattice constant of up to 4.54 (approximately corresponding to phosphorus concentrations up to 6%) can obviously be expected to be lattice-matched with said boron nitride phosphide buffer layer. Considering the teaching of matching the lattice of boron nitride phosphide layers to any crystalline layer with lattice constant between the limits as given in column 4, line 40, and considering that in the present application the overlying semiconductor layer itself is also a III-V compound semiconductor layer, hence has even more similarity with the aforementioned boron nitride phosphide buffer layer than the silicon layer in Doll et al, it is particularly obvious that the teaching by Doll et al has not only motivation (lattice matching) but also combinability with reasonable expectation of success.

10. ***Claim 8*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al, Kawai and Thornton et al as applied to claim 5 above, and further in view of Doll (5,326,424). Neither Hatano et al, Kawai, nor Thornton et al necessarily teach the further limitation defined by claim 8. However, as shown by Doll (cf. title, abstract and column 4, lines 27-40) it has long been known in the art of boron nitride phosphide films in semiconductor devices that, for the specific purpose of enabling lattice matching of boron nitride phosphide layers with overlying semiconductor crystalline substrates the phosphor content in the boron nitride phosphide layer can be varied such as to cover the range between 3.6157(10) Å and 4.5383(4) Å (cf. Otfried Madelung, "Semiconductors – Basic Data, 2nd Revised Edition, ISBN 3-540-60883-4, Springer

Verlag, Berlin Heidelberg New York 1996). Consequently, any stoichiometric value of the phosphorus content in the gallium nitride phosphide single crystal layer directly overlying the aforementioned boron nitride phosphide buffer layer that corresponds to a lattice constant of up to about 4.54 (approximately corresponding to phosphorus concentrations up to 6%) can obviously be expected to be lattice-matched with said boron nitride phosphide buffer layer. Considering the teaching of matching the lattice of boron nitride phosphide layers to any crystalline layer with lattice constant between the limits as given in column 4, line 40, and considering that in the present application the overlying semiconductor layer itself is also a III-V compound semiconductor layer, hence has even more similarity with the aforementioned boron nitride phosphide buffer layer than the silicon layer in Doll et al, it is particularly obvious that the teaching by Doll et al has not only motivation (lattice matching) but also combinability with reasonable expectation of success.

11. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al, Kawai, and Liu et al as applied to claim 4 above, and further in view of Doll et al (5,326,424). As detailed above, claim 4 is unpatentable over Hatano et al in view of Kawai and Liu et al. Neither Hatano et al nor Kawai nor Liu et al necessarily teach the further limitation as defined by claim 11. However, as we have seen from the discussion of claim 7, it is entirely obvious to limit the range of the stoichiometric parameter x defining the phosphorus concentration ratio ("compositional ratio") in the gallium nitride phosphide single crystal layer to maximally about 6%, - hence comprising substantially the range indicated in Applicant's claim, in view of the impossibility to raise the lattice

constant of the underlying boron nitride phosphide buffer layer over the upper limit of the range indicated by Doll et al: no amount nor any lack of amount, of nitrogen or phosphorus in said boron nitride phosphorus buffer layer can be selected to achieve lattice matching for values of x for which the lattice constant of the gallium nitride phosphide single crystal layer exceeds that of boron phosphide.

12. ***Claim 12*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al, Kawai, and Thornton et al as applied to claim 5, respectively, above, and further in view of Doll et al (5,326,424). Neither Hatano et al nor Kawai nor Thornton et al necessarily teach the further limitation as defined by claim 12. However, as we have seen from the discussion of claim 7, it is entirely obvious to limit the range of the stoichiometric parameter x defining the phosphorus concentration ratio ("compositional ratio") in the gallium nitride phosphide single crystal layer to maximally about 6% in view of the impossibility to raise the lattice constant of the underlying boron nitride phosphide buffer layer over the upper limit of the range indicated by Doll et al: no amount nor any lack of amount, of nitrogen or phosphorus in said boron nitride phosphorus buffer layer can be selected to achieve lattice matching for values of x for which the lattice constant of the gallium nitride phosphide single crystal layer exceeds that of pure boron phosphide.

13. ***Claims 14 and 15*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al and Kawai as applied to claim 1 above, and further in view of Isokawa et al (6,121,637). Neither Hatano et al nor Kawai necessarily teach the further limitations defined by either claims 14 and 15. However, the very purpose of the

invention essentially taught by Hatano et al and Kawai is the construction of a lamp or light source comprising the lamp, as can be gleaned from the abstract and "Field of Invention" sections in Hatano et al (cf. abstract, line 1 and column 1, lines 8-10) and as can be learned from a multitude of patents and journal publications, for instance Isokawa et al, who teach a light-emitting device (hence lamp and light source) based on a Group III-V semiconductor light-emitting element comprising a mount lead 12 and an inner lead 11 (cf. Figure 3 (a) and column 6, lines 53-61).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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JPM
June 1, 2002